Claimed is:

1. A display system adapted to display input image data received one frame at a time at an input frame rate and an input resolution on a display having an output frame rate and an output resolution, comprising:

a pixel packing circuit adapted to generate coded image data responsive to a failsafe enable signal, the coded image data being a compressed representation of the input image data; and

a pixel unpacking circuit adapted to generate output image data capable of being displayed on the display responsive to the failsafe enable signal by manipulating the coded image data.

2. The display system of claim 1 further comprising a memory adapted to store the coded image data.

3. The system of claim 1 wherein the pixel packing circuit includes:

an input terminal adapted to receive the input image data; and

a logic circuit adapted to generate the coded image data by logically manipulating the input image data.

4. The system of claim 3 wherein the input image data includes a plurality of digital image signals and wherein the logic circuit includes:

a first adder adapted to generate a first adder signal by adding the plurality of digital image signals;

a second adder adapted to generate a second adder signal by adding first and second portions of the first adder signal;

a plurality of registers coupled to the second adder and each adapted to store sequential second adder signals; and

a first plurality of comparators adapted to generate a plurality of pixel bits by comparing the second adder signal to a first threshold limit;

a second plurality of comparators adapted to compare the second adder signal to a second threshold limit; and

a logic gate adapted to generate a palette bit by logically manipulating signals output from the second plurality of comparators.

5. The system of claim 4 wherein the first and second threshold limits are programmable.

6. The system of claim 4 wherein the plurality of digital image signals include RGB image signals.

7. The system of claim 4 wherein the plurality of registers includes as many registers as there are bits in the second adder signal.

8. The system of claim 1 wherein the pixel unpacking circuit includes a multiplexer circuit adapted to generate the output image data responsive to a pixel select signal.

9. The system of claim 8 wherein the coded image data includes a plurality of pixel bits and a palette bit and wherein the multiplexer circuit includes a multiplexer and a logic gate, the multiplexer selecting one of the pixel bits responsive to the pixel select signal and the logic gate generating a logic gate output signal by logically manipulating the selected pixel bit and the palette bit.

10. The system of claim 1 wherein the failsafe enable signal includes a first and second logic states, the first logic state indicating that the input frame rate exceeds the output frame rate.

11. A system for visually displaying digital images, comprising:

input image signals provided to the system one frame at a time, the input image signals having input characteristics;

a display capable of displaying output image signals having output characteristics;

a failsafe enable adapted to identify when the input characteristics exceeds the output characteristics;

a packing circuit adapted to generate a coded signal by compressing the input image signals responsive to the failsafe enable;

a memory adapted to store the coded signal; and

an unpacking circuit adapted to generate the output image signals at the output characteristics by logically manipulating the coded signal responsive to the failsafe enable.

12. The system of claim 11 wherein the input characteristics include an input frame rate and an input resolution and wherein the output characteristics include an output frame rate and an output resolution.

13. The system of claim 11 wherein the coded signal includes a plurality of pixel bits and a palette bit and wherein the packing circuit includes:

a first adder adapted to generate a first adder signal by adding the input image signals;

a second adder adapted to generate a second adder signal by adding first and second portions of the first adder signal;

a plurality of serially connected registers coupled to the second adder, each register being adapted to store sequential second adder signals; and

a first plurality of comparators adapted to generate the plurality of pixel bits by comparing the second adder signal to a first threshold;

a second plurality of comparators adapted to generate a corresponding plurality of comparator signals by comparing the second adder signal to a second threshold; and

a logic gate adapted to generate the palette bit by logically manipulating the plurality of comparator signals.

14. The system of claim 11 wherein the coded signal includes a plurality of pixel bits and a palette bit and wherein the unpacking circuit includes:

a multiplexer adapted to select one of the plurality of pixel bits; and

a logic circuit adapted to logically manipulate the selected pixel bit with the palette bit.

15. The system of claim 11 wherein the input image signals include RGB signals representative of a color image and wherein the output image signals represent a gray scale version of the color image.

16. A failsafe circuit, comprising:

an input pixel formatter circuit adapted to receive input signals at an input frame rate

and an input resolution representative of an image and adapted to generate a coded signal representing a compressed version of the image responsive to a failsafe enable;

a memory buffer adapted to store the coded signal; and

a pixel value generator circuit adapted to generate output signals by manipulating the coded signals and providing the output signals to a display at an output frame rate and an output resolution responsive to the failsafe enable.

17. The failsafe circuit of claim 16 wherein the input pixel formatter comprises:

a first adder adapted to generate a pixel bit intensity signal by digitally adding the input signals;

a second adder adapted to generate a pixel bit upper intensity signal by adding a first portion of the pixel bit intensity signal to a second portion of the pixel bit intensity signal;

a plurality of registers adapted to store sequential upper bit intensity signals; and

a first plurality of comparators adapted to generate the plurality of pixel bits by comparing corresponding upper bit intensity signals stored in the plurality of registers to a first threshold;

a second plurality of comparators adapted to generate a corresponding plurality of comparator signals by comparing corresponding upper bit intensity signals stored in the plurality of registers to a second threshold; and

a logic circuit adapted to generate the palette bit by logically manipulating the plurality of comparator signals.

18. The failsafe circuit of claim 17 wherein the first and second thresholds are programmable.

19. The failsafe circuit of claim 17 wherein there are as many registers in the plurality of registers as there are pixel bits in the plurality of pixel bits.

20. The failsafe circuit of claim 17 wherein the input signals are RGB color signals and wherein the output signals are a gray scale version of the RGB color signals.

21. The failsafe circuit of claim 17 wherein the coded signal represents a compression of a plurality of RGB signals.

22. The failsafe circuit of claim 17 wherein the pixel value generator circuit comprises:

a multiplexer adapted to select one of the plurality of pixel bits; and

a logic circuit adapted to logically manipulate the selected pixel bit with the palette bit.

23. A method for automatically displaying digital image data having an input frame rate on a display having an output frame rate, comprising:

enabling a failsafe signal if the input frame rate exceeds the output frame rate;

compressing the image data responsive to the failsafe signal;

displaying the compressed image data; and

allowing a user to change display settings after displaying the compressed image data.

24. The method of claim 23 wherein compressing the image data includes:

receiving RGB input signals at the input frame rate, the RGB signals being representative of a color image;

generating a pixel intensity signal by summing the RGB signals;

generating an upper pixel intensity signal by summing a first and second portion of the pixel intensity signal;

repeating for a predetermined number of times receiving, generating a pixel intensity, and generating an upper pixel intensity;

storing sequential upper pixel intensity signals in a plurality of registers;

generating a plurality of pixel bits by comparing the sequentially stored upper pixel intensity signals to a low threshold;

comparing the sequentially stored upper pixel intensity signal to a high threshold; and

generating a palette bit by logically manipulating results of the comparing to the high threshold.

25. The method of claim 24 further comprising programming the low and high thresholds.

26. The method of claim 24 wherein compressing the image data comprises:

generating a coded signal with the plurality of pixel bits and the palette bit, the coded signal representing a plurality of image pixels;

storing the coded signal in a memory;

sampling the stored coded signal at a sampling rate;

selecting a pixel bit from the coded signal at the output frame rate;

logically manipulating palette bit with the selected pixel bit at the output frame rate.